



CoreLink™  
DDR2 Dynamic Memory Controller (DMC-341r1)  
**Errata Notice**

This document contains all errata known at the date of issue in releases up to and including r1p0 of PL341 AXI DDR2 Dyn Mem Ctrl, and revision r1p1 of DMC-341 AXI DDR2 DYN MEM CTRL

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- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

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## Introduction

### Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

### Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1      Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2      Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3      Behavior that was not the originally intended behavior but should not cause any problems in applications.

## Change Control

### 09 Jul 2010: Changes in Document v10

Page	Status	ID	Cat	Summary
25	Updated	720463	Cat 2	dfi_rddata_en does not request whole memory burst
32	Updated	477163	Cat 3	tWR timing not correct when (cas_latency + t_wr = 12)
33	Updated	477165	Cat 3	tWTR timing not correct when (cas_latency + t_wtr = 12)
59	Updated	715730	Doc	DII0184C DDR2 DMC (PL341) IM - requires further information on t_ctrl_delay parameter

### 12 Aug 2009: Changes in Document v9

Page	Status	ID	Cat	Summary
25	New	720463	Cat 2	dfi_rddata_en does not request whole memory burst

### 19 May 2009: Changes in Document v8

Page	Status	ID	Cat	Summary
16	Updated	569915	Cat 1	Write data mismatch on multiple outstanding transactions from same ID
20	Updated	612566	Cat 2	Illegal PRECHARGEALL - READ sequence issued to memory
21	Updated	629616	Cat 2	Refresh generated whilst in ACTIVE_PAUSE_PEND states causes system deadlock
22	Updated	642221	Cat 2	Entering self-refresh via ACTIVE_PAUSE causes system deadlock
23	New	714923	Cat 2	Possible memory protocol violation in row-bank-column mode
36	Updated	550466	Cat 3	Changing sync from synchronous to asynchronous causes error
37	Updated	630266	Cat 3	Refresh generated whilst in CONFIG state prevents PAUSE transition
38	Updated	635217	Cat 3	Possible timing violation when using ACTIVE_PAUSE, SLEEP in multi-chip configurations
39	New	643369	Cat 3	Possible tRAS violation on 1KB page 8 bank devices
58	Updated	580165	Doc	DDI0418C DDR2 DMC r0p1 TRM - invalid row_bits options in memory_cfg Register
59	New	715730	Doc	Integration Manual requires further information on t_ctrl_delay parameter
60	New	716888	Doc	Wrong release note included with the bundle

### 16 Dec 2008: Changes in Document v7

Page	Status	ID	Cat	Summary
15	Updated	454116	Cat 1	When programmed in half memory width mode, write data for WRAP transactions is lost
16	New	569915	Cat 1	Write data mismatch on multiple outstanding transactions from same ID
18	Updated	447466	Cat 2	tCKE restriction is only enforced for 2 cycles in power down mode
19	Updated	509464	Cat 2	4Gb DDR2 at 400Mhz requires t_rfc of 131 cycles, requiring an 8-bit register
20	New	612566	Cat 2	Illegal PRECHARGEALL - READ sequence issued to memory

21	New	629616	Cat 2	Refresh generated whilst in ACTIVE_PAUSE_PEND states causes system deadlock
22	New	642221	Cat 2	Entering self-refresh via ACTIVE_PAUSE causes system deadlock
27	Updated	440616	Cat 3	tRP not extended for PRECHARGEALL operations on 8-bank configurations as in JEDEC specification
28	Updated	441891	Cat 3	Reset value of schedule_faw should be t_faw - 3, as per documented usage.
29	Updated	449363	Cat 3	Write data is incorrectly stalled by cas latency dependency which can limit performance
30	Updated	457670	Cat 3	ODT not turned off for (E)MRS command
31	Updated	458900	Cat 3	tCKE restriction not enforced for active mode
32	Updated	477163	Cat 3	tWR timing not correct when (cas_latency + t_wr = 12)
33	Updated	477165	Cat 3	tWTR timing not correct when (cas_latency + t_wtr = 12)
34	Updated	503063	Cat 3	RTL generation error on AMBA Designer r2p2-00rel0
35	Updated	511763	Cat 3	Inactive cycle between write bursts to memory when cas latency is greater than 3
36	New	550466	Cat 3	Changing sync from synchronous to asynchronous causes error
37	New	630266	Cat 3	Refresh generated whilst in CONFIG state prevents PAUSE transition
38	New	635217	Cat 3	Possible timing violation when using ACTIVE_PAUSE, SLEEP in multi-chip configurations
39	New	643369	Cat 3	Possible tRAS violation on 1KB page 8 bank devices
41	Updated	430967	Doc	Asynchronous functionality incorrectly quoted as being supported
42	Updated	441893	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - Documented description of memory_width in memc_status is incorrect.
43	Updated	441894	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - Register description of t_rp and t_rcd should include allowed range of values.
44	Updated	443915	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - restriction on doing register reads at least two cycles after areset
45	Updated	449314	Doc	DII0184A PrimeCell DDR2 DMC (PL341) r0p0 IM - timing diagrams and figures are incorrect
46	Updated	452963	Doc	DDI0418A DDR2 DMC r0p0 TRM - t_ras register incorrectly documented as 4-bits in TRM, correct width is 5-bits
47	Updated	454667	Doc	DDI0418A DDR2 DMC r0p0 TRM - Incorrectly documented width for register bitfield schedule_rp
48	Updated	458968	Doc	DDI0418A DDR2 DMC r0p0 TRM - is missing qos_override signal in miscellaneous signals list
49	Updated	462541	Doc	DDI0418A DDR2 DMC r0p0 TRM - Manager FSM diagram incorrect
50	Updated	466779	Doc	DDI0418B DDR2 DMC (PL341) r0p1 TRM - Figures show incorrect timing
52	Updated	466781	Doc	DDI0418B DDR2 DMC (PL341) r0p1 TRM - No description of 'stop_mem_clock' field in mem_cfg register



53	Updated	501163	Doc	DDI0418C DDR2 DMC r0p1 TRM - Error in clock_cfg field of memory_cfg2 register
54	Updated	511073	Doc	DDI0418C DDR2 DMC r0p1 TRM - example code in Table 2-1 initialises memory_cfg2 register to an illegal value
55	Updated	511074	Doc	DDI0418C DDR2 DMC r0p1 TRM - incorrect values for t_xsr and t_esr in Table 2-1
56	Updated	520065	Doc	DDI0418C DDR2 DMC r0p1 TRM - t_rfc bitfields increased to 8-bits
57	Updated	520066	Doc	DII0184B DDR2 DMC r0p1 IM - read_delay is a 3-bit signal
58	New	580165	Doc	DDI0418C DDR2 DMC r0p1 TRM - invalid row_bits options in memory_cfg Register

**08 Apr 2008: Changes in Document v6**

Page	Status	ID	Cat	Summary
19	New	509464	Cat 2	4Gb DDR2 at 400Mhz requires t_rfc of 131 cycles, requiring an 8-bit register
35	New	511763	Cat 3	Inactive cycle between write bursts to memory when cas latency is greater than 3
57	New	520066	Doc	DII0184B DDR2 DMC r0p1 IM - read_delay is a 3-bit signal
56	New	520065	Doc	DDI0418C DDR2 DMC r0p1 TRM - t_rfc bitfields increased to 8-bits
55	New	511074	Doc	DDI0418C DDR2 DMC r0p1 TRM - incorrect values in table 2-1
54	New	511073	Doc	DDI0418C DDR2 DMC r0p1 TRM - example code initialises memory_cfg2 register to illegal value

**14 Feb 2008: Changes in Document v5**

Page	Status	ID	Cat	Summary
34	New	503063	Cat 3	RTL generation error on AMBA Designer r2p2-00rel0
53	New	501163	Doc	DDI0418C DDR2 DMC r0p1 TRM - Error in clock_cfg field of memory_cfg2 register

**22 Nov 2007: Changes in Document v4**

Page	Status	ID	Cat	Summary
33	New	477165	Cat 3	tWTR timing not correct when (cas_latency + t_wtr = 12)
32	New	477163	Cat 3	tWR timing not correct when (cas_latency + t_wr = 12)
31	Updated	458900	Cat 3	tCKE restriction not enforced for active mode
52	New	466781	Doc	DDI0418B DDR2 DMC r0p1 TRM - No description of 'stop_mem_clock' field in mem_cfg register
50	New	466779	Doc	DDI0418B DDR2 DMC r0p1 TRM - Figures show incorrect timing
47	Updated	454667	Doc	DDI0418A DDR2 DMC r0p0 TRM - Incorrectly documented width for register bitfield schedule_rp
46	Updated	452963	Doc	DDI0418A DDR2 DMC r0p0 TRM - t_ras register incorrectly documented as 4-bits in TRM, correct width is 5-bits
45	Updated	449314	Doc	DII0184A PrimeCell DDR2 DMC (PL341) r0p0 IM - timing diagrams and figures are incorrect

44	Updated	443915	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - restriction on doing register reads at least two cycles after areset
43	Updated	441894	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - Register description of t <sub>rp</sub> and t <sub>rcd</sub> should include allowed range of values.

**16 Oct 2007: Changes in Document v3**

Page	Status	ID	Cat	Summary
30	New	457670	Cat 3	ODT not turned off for (E)MRS command
31	New	458900	Cat 3	tCKE restriction not enforced for active mode
48	New	458968	Doc	DDI0418A DDR2 DMC r0p0 TRM - is missing qos_override signal in miscellaneous signals list
49	New	462541	Doc	DDI0418A DDR2 DMC r0p0 TRM - Manager FSM diagram incorrect

**14 Sep 2007: Changes in Document v2**

Page	Status	ID	Cat	Summary
15	New	454116	Cat 1	When programmed in half memory width mode, write data for WRAP transactions is lost
18	New	447466	Cat 2	tCKE restriction is only enforced for 2 cycles in power down mode
29	New	449363	Cat 3	Write data is incorrectly stalled by cas latency dependency which can limit performance
27	Updated	440616	Cat 3	tRP not extended for PRECHARGEALL operations on 8-bank configurations as in JEDEC specification
47	New	454667	Doc	Incorrectly documented width for register bitfield schedule_rp
46	New	452963	Doc	t <sub>ras</sub> register incorrectly documented as 4-bits in TRM, correct width is 5-bits
45	New	449314	Doc	Integration Manual timing diagrams and figures are incorrect
44	New	443915	Doc	Documentation should include restriction on doing register reads at least two cycles after areset
42	Updated	441893	Doc	Documented description of memory_width in memc_status is incorrect.

**12 Jun 2007: Changes in Document v1**

Page	Status	ID	Cat	Summary
28	New	441891	Cat 3	Reset value of schedule_faw should be documented and implemented as t <sub>faw</sub> - 3, as per documented usage.
27	New	440616	Cat 3	tRP not extended for PRECHARGEALL operations on 8-bank configuration
43	New	441894	Doc	Register description of t <sub>rp</sub> and t <sub>rcd</sub> should include allowed range of values.
42	New	441893	Doc	Documented description of memory_width in memc_status is incorrect.
41	New	430967	Doc	Asynchronous functionality incorrectly quoted as being supported

## Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0	r0p0-00bet1	r0p0-00rel0	r0p1-00rel0	r0p1-00rel1	r0p1-01rel0	r1p0-00rel0	r1p0-00rel1	r1p1-00rel0
430967	Doc	Asynchronous functionality incorrectly quoted as being supported	X	X							
441893	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - Documented description of memory_width in memc_status is incorrect.	X	X	X						
441894	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - Register description of t_rp and t_rcd should include allowed range of values.	X	X	X						
443915	Doc	DDI0418A DDR2 DMC (PL341) r0p0 TRM - restriction on doing register reads at least two cycles after areset	X	X	X						
449314	Doc	DII0184A PrimeCell DDR2 DMC (PL341) r0p0 IM - timing diagrams and figures are incorrect	X	X	X						
452963	Doc	DDI0418A DDR2 DMC r0p0 TRM - t_ras register incorrectly documented as 4-bits in TRM, correct width is 5-bits	X	X	X						
454667	Doc	DDI0418A DDR2 DMC r0p0 TRM - Incorrectly documented width for register bitfield schedule_rp	X	X	X						
458968	Doc	DDI0418A DDR2 DMC r0p0 TRM - is missing qos_override signal in miscellaneous signals list	X	X	X						

ID	Cat	Summary of Erratum	r0p0	r0p0-00bet1	r0p0-00rel0	r0p1-00rel0	r0p1-00rel1	r0p1-01rel0	r1p0-00rel0	r1p0-00rel1	r1p1-00rel0
462541	Doc	DDI0418A DDR2 DMC r0p0 TRM - Manager FSM diagram incorrect	X	X	X						
466779	Doc	DDI0418B DDR2 DMC (PL341) r0p1 TRM - Figures show incorrect timing				X					
466781	Doc	DDI0418B DDR2 DMC (PL341) r0p1 TRM - No description of 'stop_mem_clock' field in mem_cfg register				X					
501163	Doc	DDI0418C DDR2 DMC r0p1 TRM - Error in clock_cfg field of memory_cfg2 register	X	X	X	X	X	X			
511073	Doc	DDI0418C DDR2 DMC r0p1 TRM - example code in Table 2-1 initialises memory_cfg2 register to an illegal value	X	X	X	X	X	X			
511074	Doc	DDI0418C DDR2 DMC r0p1 TRM - incorrect values for t_xsr and t_esr in Table 2-1	X	X	X	X	X	X			
520065	Doc	DDI0418C DDR2 DMC r0p1 TRM - t_rfc bitfields increased to 8-bits				X	X	X			
520066	Doc	DII0184B DDR2 DMC r0p1 IM - read_delay is a 3-bit signal				X	X	X			
580165	Doc	DDI0418C DDR2 DMC r0p1 TRM - invalid row_bits options in memory_cfg Register				X	X	X			
715730	Doc	DII0184C DDR2 DMC (PL341) IM - requires further information on t_ctrl_delay parameter							X	X	
716888	Doc	Wrong release note included with the bundle							X		
454116	Cat 1	When programmed in half memory width mode, write data for WRAP transactions is lost	X	X	X						

ID	Cat	Summary of Erratum	r0p0	r0p0-00bet1	r0p0-00rel0	r0p1-00rel0	r0p1-00rel1	r0p1-01rel0	r1p0-00rel0	r1p0-00rel1	r1p1-00rel0
569915	Cat 1	Write data mismatch on multiple outstanding transactions from same ID						X			
447466	Cat 2	tCKE restriction is only enforced for 2 cycles in power down mode	X	X	X						
509464	Cat 2	4Gb DDR2 at 400Mhz requires t <sub>r</sub> fc of 131 cycles, requiring an 8-bit register	X	X	X	X	X				
612566	Cat 2	Illegal PRECHARGEALL - READ sequence issued to memory	X	X	X	X	X	X			
629616	Cat 2	Refresh generated whilst in ACTIVE_PAUSE_PEND states causes system deadlock				X	X	X			
642221	Cat 2	Entering self-refresh via ACTIVE_PAUSE causes system deadlock	X	X	X	X	X	X			
714923	Cat 2	Possible memory protocol violation in row-bank-column mode	X	X	X	X	X	X			
720463	Cat 2	dfi_rddata_en does not request whole memory burst							X	X	
440616	Cat 3	tRP not extended for PRECHARGEALL operations on 8-bank configurations as in JEDEC specification	X	X	X						
441891	Cat 3	Reset value of schedule_faw should be t <sub>faw</sub> - 3, as per documented usage.	X	X	X						
449363	Cat 3	Write data is incorrectly stalled by cas latency dependency which can limit performance	X	X	X						
457670	Cat 3	ODT not turned off for (E)MRS command	X	X	X						
458900	Cat 3	tCKE restriction not enforced for active mode	X	X	X						

ID	Cat	Summary of Erratum	r0p0	r0p0-00bet1	r0p0-00rel0	r0p1-00rel0	r0p1-00rel1	r0p1-01rel0	r1p0-00rel0	r1p0-00rel1	r1p1-00rel0
477163	Cat 3	tWR timing not correct when (cas_latency + t_wr = 12)	X	X	X	X	X	X	X	X	
477165	Cat 3	tWTR timing not correct when (cas_latency + t_wtr = 12)	X	X	X	X	X	X	X	X	
503063	Cat 3	RTL generation error on AMBA Designer r2p2-00rel0	X	X	X	X					
511763	Cat 3	Inactive cycle between write bursts to memory when cas latency is greater than 3	X	X	X	X	X				
550466	Cat 3	Changing sync from synchronous to asynchronous causes error				X	X	X			
630266	Cat 3	Refresh generated whilst in CONFIG state prevents PAUSE transition				X	X	X			
635217	Cat 3	Possible timing violation when using ACTIVE_PAUSE, SLEEP in multi-chip configurations	X	X	X	X	X	X			
643369	Cat 3	Possible tRAS violation on 1KB page 8 bank devices	X	X	X	X	X	X			

## Errata - Category 1

### **454116: When programmed in half memory width mode, write data for WRAP transactions is lost**

#### **Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 1, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

#### **Description**

The PL341 controller has the option to be programmed for use with memory devices half the configured width of the memory interface.

The defect causes the controller to corrupt data written to memory as part of WRAP type AXI transactions when used in this mode.

#### **Implications**

The controller cannot reliably be used to write data to memory devices half the configured width using WRAP type AXI transactions.

When used with memory devices of width equal to the configured memory width, or if performing writes using INCR or FIXED type AXI transactions, this defect will not effect operation.

#### **Workaround**

na

**569915: Write data mismatch on multiple outstanding transactions from same ID****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 1, Present in: r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

If the PL341 Dynamic Memory Controller has three or more write transactions with the same AXI ID active in its queue, a certain condition exists under which it will incorrectly match incoming write data to the wrong queue entry.

The condition under which this occurs can be summarised as follows:

- 1) Three or more transactions of the same AXI ID are active in the queue
- 2) The last data beat for the oldest transaction is received by the controller
- 3) Then the AXI write channel is idle for a specific number of cycles. The number of cycles must be such that when the last data beat is pushed into the write buffer, there is a gap of exactly one cycle before the subsequent beat is processed in the axiwiif block.
- 4) The first data beat for the second transaction is received by the controller.

Under this condition, the first beat of the second transaction is incorrectly associated with the third write transaction.

**Implications**

If write data is associated with the incorrect queue entry, data corruption and deadlock can occur.

**Workaround**

Limiting each master in the system to one or two outstanding write transactions will mean this defect will never be observed. Similarly, limiting the total number of outstanding write transactions to one or two will mean this defect will never be observed.





## Errata - Category 2

### **447466: tCKE restriction is only enforced for 2 cycles in power down mode**

#### **Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 2, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

#### **Description**

The JEDEC standard specifies a timing parameter tCKE, which is defined as the minimum allowed time a device can spend in power down mode.

For some devices, this parameter is 3 cycles. PL341 only enforces a minimum of 2 cycles.

#### **Implications**

If the PL341 controller is used with a device that requires tCKE=3, and the auto power down feature is enabled, the tCKE restriction will potentially be violated.

This could cause data corruption in the memory.

#### **Workaround**

To ensure safe operation, disable the auto power down feature using the auto\_power\_down bit of the memory configuration register.

**509464: 4Gb DDR2 at 400Mhz requires t<sub>rfc</sub> of 131 cycles, requiring an 8-bit register****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 2, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1, Fixed in r0p1-01rel0.

**Description**

The JEDEC specification states t<sub>RFC</sub> for a 4Gb device is 327.5ns

At a clock speed of 400Mhz, this translates to 131 clock cycles.

The t<sub>rfc</sub> register field, being 7 bits, supports a maximum of 127 cycles.

**Implications**

The JEDEC specification states: If refresh timing is violated, data corruption may occur.

Therefore, this defect implies it is not safe to use a 4Gb device at 400Mhz.

**Workaround**

N/A

**612566: Illegal PRECHARGEALL - READ sequence issued to memory****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 2, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

There is a corner case condition under which the DMC issues a PRECHARGEALL followed by a READ command.

For this case to occur, the sequence of events is:

- 1) The configuration is a multi-chip design
- 2) The queue has no memory operations ready for arbitration
- 3) An AUTOREFRESH is scheduled for one of the active chips
- 4) A PRECHARGEALL is required to close open rows within that chip
- 5) In the cycle in which the PRECHARGEALL is pushed onto the command FIFO, a read transaction to the same chip, bank, and previously active row enters the queue into an entry which previously contained a command to a different chip.

Under these circumstances, the read is arbitrated in the next cycle and causes the issue to occur.

**Implications**

The READ command will be sent to an inactive bank in the memory device, which could result in system failure.

**Workaround**

In single chip configurations, this defect will not occur.

In multi-chip configurations, programming refresh\_timeout to 1 will prevent the read from being arbitrated after the PRECHARGEALL.

**629616: Refresh generated whilst in ACTIVE\_PAUSE\_PEND states causes system deadlock****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 2, Present in: r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

The controller provides an ACTIVE\_PAUSE feature which allows entry into low power state without waiting for an idle system.

Whilst transitioning from READY to PAUSE using this method, there are two cycles during which the pipeline is checked for any new AXI accesses. These are the ACTIVE\_PAUSE\_PEND states.

Should an AUTOREFRESH happen to be scheduled during one of these two cycles, the state machine will not advance, but also the refresh will not be arbitrated.

**Implications**

Under these circumstances the state machine will not transition to PAUSE state and will remain in the pending state indefinitely.

**Workaround**

Use the PAUSE command to transition to PAUSE state instead of the ACTIVE\_PAUSE command.

**642221: Entering self-refresh via ACTIVE\_PAUSE causes system deadlock****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 2, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

The ACTIVE\_PAUSE command will allow the controller to transition to PAUSE state without first emptying the queue.

In order to allow subsequent transition into LOW\_POWER state one slot in the queue must be left empty to allow the manager block to issue a SELFREFRESHENTRY command.

The ACTIVE\_PAUSE\_PEND internal states of the manager state machine are intended to cater for the corner case when an AXI transaction is accepted (and fills the queue) during this transition.

A corner case exists where the following sequence occurs:

- 1) Queue has exactly two empty slots
- 2) The ACTIVE\_PAUSE command is given
- 3) Two AXI transactions (one read, one write) are received in the last cycle of the READY state

In this scenario, the two AXI transactions are both accepted into the queue during the two PEND states and the state transition to PAUSE takes place concurrently with the queue becoming full.

**Implications**

In the described scenario, the controller is left in the PAUSE state, with a full queue.

If the SLEEP command is then given, this command cannot be accepted by the queue and the system will deadlock.

**Workaround**

None. Alternative methods for entry to LOW\_POWER must be used if the conditions above cannot be avoided.

## 714923: Possible memory protocol violation in row-bank-column mode

### Status

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 2, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

### Description

If a single AXI transaction crosses a page boundary it will cause a column overflow. When in row-bank-column mode, the resulting memory accesses will increment into the next bank.

If the following sequence of events should occur, it is possible for the PL341 memory controller to issue a PRECHARGE-MEMOP sequence to a bank in violation of the memory protocol.

- 1) An AXI transaction is decoded using row/bank/column addressing
- 2) The row address is open in the bank (bank+1)
- 3) The AXI access increments out of the starting page, causing a column overflow. It will subsequently address (bank+1), where it will be an open-row hit.
- 4) In the cycle immediately after the last access to the original page, another queue entry causes a PRECHARGE command to be sent to (bank+1), closing the open row.
- 5) The original entry is arbitrated in the next cycle, but has not had its page table updated and so is incorrectly marked as a hit. The MEMOP command occurs and violates protocol.

Note that an AXI access will never cross a 4KB boundary. Individual masters may have further restrictions on the AXI address boundaries they will and will not cross.

To determine the memory page size with respect to the system address map, use the following formula:

PageSize = 1 << (memory\_width+1+column\_bits+8)

Where memory\_width is the value programmed in the memory\_cfg2 register, and column\_bits is the value programmed in the memory\_cfg register.

### Implications

Under the described scenario, a memory protocol violation will occur with unpredictable results.

This protocol violation will take the form of a READ/WRITE command occurring whilst the memory is in the PRECHARGING or IDLE state.

For a write, it is likely the data will be lost. For a read, the returned data is likely to be corrupted.

### Workaround

This scenario will not occur if using bank-row-column addressing. To use Bank-row-column addressing, program the brc\_n\_rbc bit of the chip\_<n>\_cfg register to 1'b1, as documented in the PL341 technical reference manual.

Note that the choice of addressing mode may affect the system performance depending on the profile of the memory traffic.



**720463: dfi\_rddata\_en does not request whole memory burst****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 2, Present in: r1p0-00rel0,r1p0-00rel1, Fixed in r1p1-00rel0.

**Description**

The DMC can be configured to use a DFI interface to connect to the PHY.

There is a defect in the implementation of the dfi\_rddata\_en signal; dfi\_rddata\_en is only asserted for the number of beats of data the DMC requires.

The DFI specification is ambiguous in the useage of this signal, however we understand that the intent of the signal is to be asserted for all of the beats of a requested burst.

Consider a 32 bit AXI controller with a 16 bit memory interface.

Assume the memory is setup in burst length 4 (4 x 16 bit data beats).

The DMC may only require one or two beats of the burst if a 16 bit or 32 bit AXI single is requested.

The DMC will only assert the dfi\_rddata\_en signal for one cycle, on which two beats of the burst are presented by the PHY.

The intent of the DFI spec is that dfi\_rddata\_en is always asserted for two cycles so all four beats of the burst are presented by the PHY.

The resulting behaviour will depend on the implementation of the specific PHY.

This defect will only arise when the AXI requests less data than the programmed memory burst length.

**Implications**

The implications of this defect will depend on the specific PHY implementation.

There is likely to be a data error.

Possibilities include:

- Data error when PHY fails to capture any data for the requested burst
- Data error when PHY fails to capture part of the requested burst
- Data error in following burst when PHY presents unrequired beats of previous burst

**Workaround**

There are no software workarounds.

However, this defect will not occur if the system designer can ensure that all AXI requests are for complete multiples of a programmed memory burst of data.



## Errata - Category 3

### **440616: tRP not extended for PRECHARGEALL operations on 8-bank configurations as in JEDEC specification**

#### **Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

#### **Description**

The JEDEC specification for DDRII devices states that, for an 8-bank device, tRP must be extended by one memory clock cycle following a PRECHARGEALL operation.

The PL341 controller does not extend tRP in this way.

#### **Implications**

The controller will only delay subsequent commands by the programmed t<sub>rp</sub> number of cycles. If this delay is not sufficient for the memory device in use, then some memory corruption may occur.

#### **Workaround**

The workaround for this issue would be to program the t<sub>rp</sub> register to the maximum required value, that is tRP + 1.

This would force the controller to insert the required delay. Note that this will mean all PRECHARGE operations will incur an additional cycle latency if tRP is an even value.

**441891: Reset value of schedule\_faw should be t\_faw - 3, as per documented usage.****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

The register description for the t\_faw register describes the bitfield schedule\_faw as needing to be programmed to t\_faw - 3. The reset value of the register, however, is currently documented and implemented as equal to t\_faw.

**Implications**

The current setting of this register will not cause any functional problems. There may be an occasional performance penalty if the register is not re-programmed by the User as the arbitration uses the scheduler to delay arbitrating further commands until the schedule counter expires.

**Workaround**

It is intended that the User programs the register to the required value during initial configuration. The documented usage of programming t\_faw - 3 should be followed.

**449363: Write data is incorrectly stalled by cas latency dependency which can limit performance****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

DDRII memory supports seamless burst write operation, whereby write data can be transferred on every cycle.

PL341 incorrectly implements a dependency on the cas latency for issue of write data. That is, a new write burst is not started if a previous command was issued within (cas\_latency - 1) cycles.

**Implications**

This limitation can impair write performance in applications that require write data streaming when cas latency is more than 3 cycles.

**Workaround**

Use memories that support cas latency of 3 cycles.

**457670: ODT not turned off for (E)MRS command****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

The Jedec DDRII specification states that the ODT signal must be deasserted low prior to performing an EMRS command.

The PL341 memory controller does not enforce this condition.

**Implications**

If the system uses ODT, and the EMRS register is modified after initialisation, the PL341 controller does not guarantee the ODT signal is deasserted prior to performing the EMRS command.

ODT is required to be OFF for EMRS commands, to prevent impedance glitches on the channel.

The state of the ODT signal will be determined by the previous command(s) executed on the interface. For a system with a single active chip ODT is asserted for writes, and deasserted for reads and self-refresh entry. For a system with multiple active chips, ODT is deasserted for a chip during an access to that chip, and re-asserted when an access to another chip occurs.

**Workaround**

To ensure ODT is deasserted for an EMRS command, perform a self-refresh entry prior to executing the required command sequence.

**458900: tCKE restriction not enforced for active mode****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

The Jedec specification for DDR2 dictates a tCKE minimum timing restriction for pulses of the CKE signal.

The PL341 memory controller does not enforce the minimum high tCKE restriction.

**Implications**

Because the controller does not enforce the tCKE restriction, CKE intensive applications may result in violation of this timing restriction.

For example, consider the case when the controller has put a memory device into power-down mode by deasserting CKE. The controller will power up the device by asserting CKE in order to issue the next command. If the next command is a self-refresh command then CKE will not remain asserted for the required tCKE period before CKE is deasserted to enter self-refresh.

**Workaround**

There are two workarounds to this problem:

- 1) Do not enable the auto power down feature
- 2) Program t<sub>xp</sub> to be greater than tCKE, as the controller will not issue the self refresh command with t<sub>xp</sub> cycles of exiting power down state

**477163: tWR timing not correct when (cas\_latency + t\_wr = 12)****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0,r1p0-00rel0,r1p0-00rel1, Fixed in r1p1-00rel0.

**Description**

tWR governs the write recovery time, and is a minimum timing requirement according to the JEDEC DDR2 specification.

This defect means that when the programmed values of cas\_latency and t\_wr add up to twelve, the observed tWR delay is one less than expected.

**Implications**

If the User has programmed these values then the tWR timing parameter could be violated by the controller. If this occurs the memory device will enter an error state.

**Workaround**

Programming the values so they do not add to twelve will ensure this defect is not observed.



**477165: tWTR timing not correct when (cas\_latency + t\_wtr = 12)****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0,r1p0-00rel0,r1p0-00rel1, Fixed in r1p1-00rel0.

**Description**

tWTR governs the write to read command time, and is a minimum timing requirement according to the JEDEC DDR2 specification.

This defect means that when the programmed values of cas\_latency and t\_wtr add up to twelve, the observed tWTR delay is one less than expected.

**Implications**

If the User has programmed these values then the tWTR timing parameter could be violated by the controller. If this occurs the memory device will enter an error state.

**Workaround**

Programming the values so they do not add to twelve will ensure this defect is not observed.

**503063: RTL generation error on AMBA Designer r2p2-00rel0****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0, Fixed in r0p1-00rel1.

**Description**

AMBA Designer is intended to be the configuration tool for PL341. In order to use AMBA Designer a plug-in must be present in the configuration scripts part.

This plug-in is not present in releases up to and including r0p1\_00rel0

**Implications**

AMBA Designer cannot be used to configure these releases of PL341.

**Workaround**

A makefile is provided to enable customers to render a PL341 configuration without using AMBA Designer.

This method of configuration will not be supported once the AMBA Designer plug-in is released.

**511763: Inactive cycle between write bursts to memory when cas latency is greater than 3****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1, Fixed in r0p1-01rel0.

**Description**

The timing checks in the memory interface of PL341 incorrectly enforce a cycle of inactivity on the data bus between write bursts to memory when the cas latency is programmed to a value greater than 3.

**Implications**

There is a performance penalty as a cycle is inserted between bursts to DDR2 memory.

**Workaround**

None.

**550466: Changing sync from synchronous to asynchronous causes error****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p1-00rel0, r0p1-00rel1, r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

The DMC provides a register bitfield which indicates if the clock domains are synchronous or asynchronous. If this bitfield is changed from synchronous to asynchronous following a period of use, the command FIFO pointers can temporarily become incorrect.

**Implications**

If the FIFO pointers become unaligned when the sync bit is changed then erroneous commands may be sent over the memory interface which could cause failures including a system deadlock.

**Workaround**

The problem can be worked around by issuing a number of NOP commands equal (or greater) than the length of the Command FIFO before changing the sync bit. This will ensure that any inconsistency between the pointers will have no functional effect

**630266: Refresh generated whilst in CONFIG state prevents PAUSE transition****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p1-00rel0, r0p1-00rel1, r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

The technical reference manual describes the transition between CONFIG and PAUSE states via the issue of an APB command PAUSE.

Periodic AUTOREFRESH commands are scheduled via the refresh logic inside the controller. These commands are not arbitrated by the controller whilst in CONFIG state, to avoid interference with software controlled programming operations. However, the transition from CONFIG to PAUSE state checks that the refresh queue is empty. Therefore, if a new refresh enters the queue between the last software-generated refresh and the PAUSE command this transition will not take place.

**Implications**

In the described scenario a system deadlock could occur.

**Workaround**

To transition from CONFIG to PAUSE state safely, do a command sequence: GO, PAUSE.

## **635217: Possible timing violation when using ACTIVE\_PAUSE, SLEEP in multi-chip configurations**

### **Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

### **Description**

The memory controller is responsible for ensuring that any commands generated as a result of system stimulus comply with the inter-command timings as documented in the Technical Reference Manual.

The APB command SLEEP cause the controller to issue:

a PRECHARGEALL command (if any banks are open in any chip)

a SELFREFRESHENTRY command

These commands are issued to all chips simultaneously to reduce power.

However, the logic that checks timing for these commands is incorrectly checking that timing is met for any chip, not all chips.

For example, in a 2-chip system consider the following sequence:

An AXI transaction prepares a bank by issuing an ACTIVATE command to chip 1. The tRAS timing parameter now precludes further commands from occurring until it has expired.

An APB request to ACTIVE\_PAUSE moves the controller into the PAUSED state.

An APB request to SLEEP causes a PRECHARGEALL command to be issued.

Since there has been no recent activate to chip 0, the command is enabled for chip 0. However, it is also incorrectly sent to chip 1, in violation of the tRAS parameter.

Note this situation can only occur if:

There are two or more active chips

The ACTIVE\_PAUSE command is used to initiate the sequence

The SLEEP command is used

The programmed timing parameters are longer than the software requests ACTIVE\_PAUSE to SLEEP.

### **Implications**

Under the scenario described, the controller will issue commands that do not observe the required inter-command timings.

Such behaviour may cause unpredictable response from the memory device.

### **Workaround**

To ensure timing parameters are not violated, the software controlling the ACTIVE\_PAUSE, SLEEP sequence should wait in PAUSED state enough cycles for all timing parameters to expire.

**643369: Possible tRAS violation on 1KB page 8 bank devices****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Cat 3, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

The JEDEC specification describes the tRAS timing parameter which governs the minimum delay between ACTIVATE and PRECHARGE commands to the same bank.

In the PL341 controller the control logic for this timing parameter is implemented as four counters for each chip which track the time since the last ACTIVATE.

If more than four ACTIVATE commands are issued in less than tRAS, these counters can incorrectly be overloaded with the new bank information which may lead to a tRAS timing violation.

For eight bank memories the parameter tFAW restricts the timing window within which a maximum of four ACTIVATE commands can be issued.

The tRRD timing parameter defines the minimum ACTIVATE to ACTIVATE command time.

The relationships between these timing parameters mean that for DDR2-667 and DDR2-800 1KB page devices with 8 banks, tFAW and tRRD do not offer protection from issuing more than four ACTIVATE commands within tRAS. For these devices, the PL341 controller may violate the tRAS parameter.

**Implications**

If using DDR2-667 or DDR2-800 devices with a 1KB page size and eight banks, the PL341 controller may violate the tRAS timing parameter.

**Workaround**

In order to prevent this from occurring, ensure that one of the following statements is true:

t\_rrd is programmed to be greater than or equal to t\_ras divided by 4

t\_faw is programmed to be greater than or equal to t\_ras





## Errata - Documentation

### **430967: Asynchronous functionality incorrectly quoted as being supported**

#### **Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1, Fixed in r0p0-00rel0.

#### **Description**

Section 1.1.1 of the TRM refers to asynchronous interfaces in the device. Although these are present in the device, they are not currently part of the validated and released product functionality and so these sections of the TRM should be ignored.

#### **Implications**

None

#### **Workaround**

None

**441893: DDI0418A DDR2 DMC (PL341) r0p0 TRM - Documented description of memory\_width in memc\_status is incorrect.****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

In the Technical Reference Manual, the description of the Memory Controller Status Register (Section 3.3.1) states that the memory\_width bitfield returns the effective width of the memory interface.

The register returns the physical width of the memory interface.

**Implications**

The value returned by the register will not match the documented value.

**Workaround**

Not applicable.

**441894: DDI0418A DDR2 DMC (PL341) r0p0 TRM - Register description of t<sub>rp</sub> and t<sub>rcd</sub> should include allowed range of values.**

**Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

The schedule\_x bitfields of these registers are used by the scheduler to affect arbitration decisions. These bitfields can only support values 0-4.

**Implications**

If the bitfields are programmed outside of this range then the scheduling logic could fail. This means the controller will not arbitrate selectively and pipeline stalls could occur.

**Workaround**

Not Applicable.

**443915: DDI0418A DDR2 DMC (PL341) r0p0 TRM - restriction on doing register reads at least two cycles after areset****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

In the Technical Reference Manual in Figure 2-3 "clk domain state diagram" it is indicated that, following Power-On-Reset (POR), there are two state transitions to enter the CONFIG state.

Registers cannot be read or written to during these two clock cycles as the controller is not yet considered to be in the CONFIG state.

**Implications**

This restriction should be clarified, as otherwise a User might attempt to program or read from a register as part of an initialisation sequence.

**Workaround**

na

**449314: DII0184A PrimeCell DDR2 DMC (PL341) r0p0 IM - timing diagrams and figures are incorrect****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

The Integration Manual has the following defects:

Page 2-15: The table and text describing read path delays has unsuitable values for DDRII. Please refer to the memory device data sheet and your synthesis flow for realistic timings.

**Implications**

The timings in the example are unsuitable for use with DDRII designs.

**Workaround**

na

**452963: DDI0418A DDR2 DMC r0p0 TRM - t\_ras register incorrectly documented as 4-bits in TRM, correct width is 5-bits****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

In the Technical Reference Manual, under section "3.3.9 t\_ras Register":

[3:0] t\_ras

This should be written as:

[4:0] t\_ras

**Implications**

The document does not reflect the design. In the event a User needed to program a value of 16 or higher, the documentation would mislead them into thinking it was not possible.

If the User had written 1'b1 to bit [4] thinking it was unused, it could cause undefined behaviour.

**Workaround**

na

**454667: DDI0418A DDR2 DMC r0p0 TRM - Incorrectly documented width for register bitfield schedule\_rp****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

The Technical Reference Manual states under "Table 3-14 t\_rp Register bit assignments":

[11:8] schedule\_rp

However, the schedule\_rp bitfield is a 3-bit field occupying [10:8]

**Implications**

If bit [11] of this register is written to, this bit is ignored.

Due to the range of values anticipated for schedule\_rp, this bit of the register does not need to be programmed to 1'b1.

**Workaround**

na

**458968: DDI0418A DDR2 DMC r0p0 TRM - is missing qos\_override signal in miscellaneous signals list****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

In section A-2 of the technical reference manual, the miscellaneous signals table does not show the 16-bit qos\_override input signal.

**Implications**

The PL341 controller has a 16-bit input signal qos\_override, which must be connected correctly when used in a system.

The purpose of the signal is described elsewhere in the document.

**Workaround**

N/A



**462541: DDI0418A DDR2 DMC r0p0 TRM - Manager FSM diagram incorrect****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0, Fixed in r0p1-00rel0.

**Description**

Figure 2-3 clk domain state diagram

This diagram shows a transition from the Config state to the Low power state using the sleep command.

This transition is not a valid state transition.

**Implications**

If this transition is attempted, the hardware will silently fail (ignore) the command and remain in the Config state.

**Workaround**

N/A

**466779: DDI0418B DDR2 DMC (PL341) r0p1 TRM - Figures show incorrect timing****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

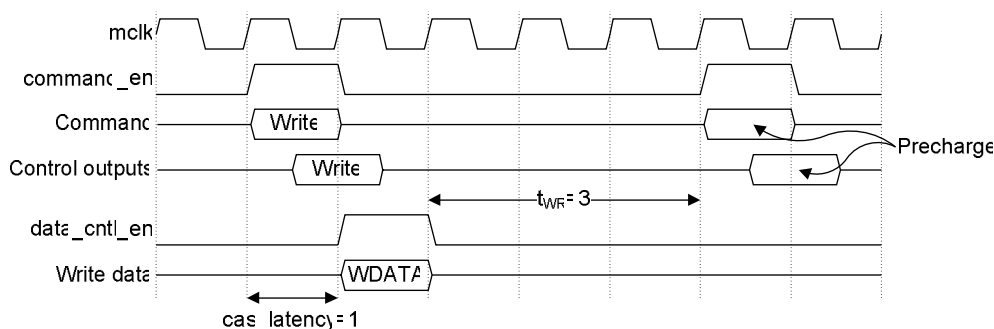
Fault status: Doc, Present in: r0p1-00rel0, Fixed in r0p1-00rel1.

**Description**

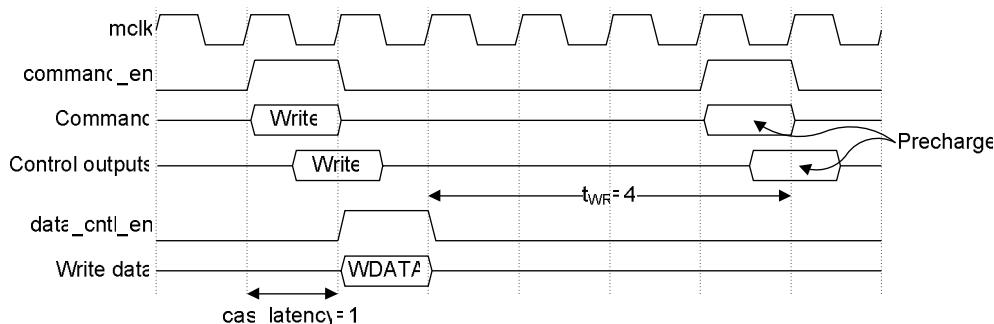
Some of the timing diagrams in the the Technical Reference Manual do not show correctly how a timing parameter is applied.

The numerical value shown for the timing paramater does not correspond with the timing of the signals shown in the diagrams. In each case, the numerical value should be one higher than the timing shown, and the arrow should be extended to the next rising clock edge.

For example the existing diagram Figure 2-19:



Should be displayed as:



The figures affected by this defect are as follows:

Figure 2-9 Activate to read or write command timing,  $t_{RCD}$

Figure 2-11 Bank activate to bank activate or auto-refresh command timing,  $t_{RC}$

Figure 2-12 Bank activate to different bank activate for a memory timing,  $t_{RRD}$

Figure 2-13 Precharge to command and auto-refresh timing,  $t_{RP}$  and  $t_{RFC}$

Figure 2-14 Activate to precharge, and precharge to precharge timing,  $t_{RAS}$  and  $t_{RP}$

Figure 2-16 Self-refresh entry and exit timing,  $t_{ESR}$  and  $t_{XSR}$

Figure 2-17 Power down entry and exit timing,  $t_{XP}$

Figure 2-18 Data output timing, tWTR

Figure 2-19 Data output timing, write latency = 2

### **Implications**

To achieve the waveform shown in the timing diagram, the User would need to program the timing register to a value one cycle longer than that indicated in the diagram.

### **Workaround**

NA

**466781: DDI0418B DDR2 DMC (PL341) r0p1 TRM - No description of 'stop\_mem\_clock' field in mem\_cfg register****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p1-00rel0, Fixed in r0p1-00rel1.

**Description**

PL341 r0p1 implements a feature to stop the memory clock when the controller is put into low power state. This feature can be enabled by setting bit 14 of the Memory Configuration Register to '1'.

The r0p1 Technical Reference Manual documents this bit as being reserved. The description should read:

stop\_mem\_clock : When enabled, the memory clock is dynamically stopped following entry into self-refresh.

**Implications**

The r0p1 documentation instructs the User to always set this bit to zero. This will leave the feature disabled and the memory clock will not be dynamically stopped.

**Workaround**

na

**501163: DDI0418C DDR2 DMC r0p1 TRM - Error in clock\_cfg field of memory\_cfg2 register****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

Table 3-21 needs to be corrected.

The description for field [1:0] should be changed such that it says the following:

Encodes the clocking scheme:

b00 = aclk and mclk are asynchronous

b01 = aclk and mclk are synchronous (This setting covers these situations: aclk < mclk, aclk > mclk, aclk = mclk)

b10 = reserved

b11 = reserved

**Implications**

The current documentation suggests that bit[1] of the register field must be set to 1'b1 in systems where the clocks are n:1 (n>1).

Attempting to set this bit will have no effect. Software checking the register may read back an unexpected value if an attempt to set it to 1'b1 has been made.

**Workaround**

For bit[1] : write as zeros, read undefined.

**511073: DDI0418C DDR2 DMC r0p1 TRM - example code in Table 2-1 initialises memory\_cfg2 register to an illegal value****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

In table 2-1 of the Technical Reference Manual, the register at register address 0x8000004C is set to 0x00000411.

This value is illegal as described in the register description section. The example value should be changed to 0x00000001.

**Implications**

The example sequence is provided as a guide to the steps required for programming the controller. The necessary values will need to be determined by the end User, however inconsistencies in the documentation may lead to confusion.

**Workaround**

N/A

**511074: DDI0418C DDR2 DMC r0p1 TRM - incorrect values for t\_xsr and t\_esr in Table 2-1****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p0,r0p0-00bet1,r0p0-00rel0,r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

In the Technical Reference Manual, in table 2-1, the following lines should be changed from:

0x80000044 0x00000003 Set t\_xsr to 3

0x80000048 0x000000c8 Set t\_esr to 200

to

0x80000044 0x000000c8 Set t\_xsr to 200

0x80000044 0x00000003 Set t\_esr to 3

**Implications**

This table shows an example initialisation sequence. The correct values to be programmed will need to be determined for each system, however the values shown may mislead the Programmer as to the functionality of the registers in question.

**Workaround**

n/a

**520065: DDI0418C DDR2 DMC r0p1 TRM - t\_rfc bitfields increased to 8-bits****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

In section 3.3.12 t\_rfc Register:

The two bitfields of this register are both 8-bits wide. The bit assignments should be amended to read:

[15:8] schedule\_rfc

[7:0] t\_rfc

**Implications**

The document currently states to program the modified bit(s) to zero, under which circumstances the IP will behave as documented.

**Workaround**

N/A



**520066: DII0184B DDR2 DMC r0p1 IM - read\_delay is a 3-bit signal****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

In Table 2-1 the signal read\_delay should be modified to indicate the signal width is 3-bits.

**Implications**

When modifying the pad interface, the correct bit width should be used otherwise errors may be seen in the design flow.

**Workaround**

N/A

**580165: DDI0418C DDR2 DMC r0p1 TRM - invalid row\_bits options in memory\_cfg Register****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r0p1-00rel0,r0p1-00rel1,r0p1-01rel0, Fixed in r1p0-00rel0.

**Description**

In Table 3-5 the valid encodings for the row\_bits are documented. In this version of the document, ranges 11-16 are documented. However, the valid range is 13-16 as per the JEDEC specification for DDR2 memories.

The table should be amended to reflect the valid range, and a note added to state that only the JEDEC-specified combinations of row bits and column bits are supported.

**Implications**

If any of the illegal values are programmed into the controller, unexpected memory access behaviour will be observed.

It is not expected that the unsupported values will be used as they fall outside the JEDEC specification for DDR2 devices.

**Workaround**

N/A

**715730: DII0184C DDR2 DMC (PL341) IM - requires further information on t\_ctrl\_delay parameter****Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r1p0-00rel0,r1p0-00rel1, Fixed in r1p1-00rel0.

**Description**

Table 2-3 of the Integration Manual details the PL341 support for DFI timing parameters.

For the t\_ctrl\_delay parameter, extra software consideration should be made to ensure that the status of the controller matches that of the memory when t\_ctrl\_delay > 1.

Software must wait t\_ctrl\_delay cycles after reading an update in the memc\_status register before taking any action that may effect the memory only permitted in the new state.

For example; if entering Low\_Power to adjust the memory clock frequency then on entry to Low\_Power state the controller will update its state once the command has been sent to the PHY. The system must wait t\_ctrl\_delay cycles to allow the SELFREFRESH command to propagate to the memory before altering the clock.

**Implications**

If the PHY delay is not taken into consideration, then the controller status may not match that of the memory.

In the example given, if the clock is removed before the device enters self-refresh then data loss may occur.

**Workaround**

NA

## **716888: Wrong release note included with the bundle**

### **Status**

Affects: product DMC-341 AXI DDR2 DYN MEM CTRL .

Fault status: Doc, Present in: r1p0-00rel0, Fixed in r1p0-00rel1.

### **Description**

The product bundle was released with an incorrect release note within it.

### **Implications**

The supplied release note does not relate to this release and so is misleading.

### **Workaround**

This issue can be worked around by either downloading an updated bundle or downloading just the updated release note.



## Errata – Driver Software

**There are no Errata in this Category**